IN THE CLAIMS

1. (Currently Amended) A method of providing access to a bus, comprising:

receiving a request for device access to the bus;

selecting the request according to a priority associated with the request;

generating a control signal in response to selection of the request;

enabling a switch associated with the request to couple a device associated with the request ~~provide access~~ to the bus in response to the control signal.

2. (Original) The method of Claim 1, wherein the bus is a PCI bus.

3. (Original) The method of Claim 2, wherein the PCI bus operates at a frequency of at least 66 MHz.

4. (Original) The method of Claim 1, wherein the request is received from a device desiring to communicate over the bus.

5. (Currently Amended) The method of Claim 1, further comprising:

receiving a plurality of device access requests for the bus, each of the plurality of device access requests being received from one of a plurality of devices not coupled to the bus, each of the plurality of devices having a switch associated therewith;

selecting a particular one of the plurality of device access requests according to a predetermined priority protocol;

generating a control signal corresponding to the selected particular one of the plurality of device access requests;

providing the control signal to a particular one of the plurality of devices that sent the selected particular one of the plurality of device access requests, the control signal enabling the switch associated with the particular one of the plurality of devices to ~~provide access~~ couple the particular one of the plurality of devices to the bus.

6. (Currently Amended) The method of Claim 5, further comprising:

selecting a next one of the plurality of device access requests according to the predetermined priority protocol;

generating a control signal corresponding to the selected next one of the plurality of device access requests;

providing the control signal to a next one of the plurality of devices that sent the selected next one of the plurality of device access requests, the control signal enabling the switch associated with the next one of the plurality of devices to ~~provide access~~ couple the next one of the plurality of devices to the bus prior to an end of ~~access~~

~~to the bus for~~ the particular one of the plurality of devices being coupled to the bus.

7. (Currently Amended) The method of Claim 6, further comprising:

determining an end ~~of access to the bus~~ for the particular one of the plurality of devices to be coupled to the bus;

initiating ~~access to the bus by~~ coupling of the next one of the plurality of devices to the bus in response to the end ~~of access to the bus~~ for the particular one of the plurality of devices to be coupled to the bus.

8. (Currently Amended) The method of Claim 7, further comprising:

generating a disabling control signal in response to the end ~~of access to the bus~~ for the particular one of the plurality of devices to be coupled to the bus;

decoupling ~~preventing~~ the particular one of the plurality of devices from ~~accessing~~ the bus in response to the disabling control signal.

9. (Original) The method of Claim 1, further comprising:

limiting a number of generated control signals in order to control a load on the bus.

Currently Amended

10. (~~Original~~) The method of Claim 1, further comprising:

generating a disable control signal for a request not selected in order to prevent coupling of an associated device ~~disable access~~ to the bus.

11. (Currently Amended) A system for providing access to a bus, comprising:

a bus controller;

a plurality of processing devices capable of being coupled to the bus controller by a bus;

a plurality of enabling switches on the bus, each enabling switch coupled to a corresponding processing device, each enabling switch determining whether ~~providing~~ the corresponding processing device ~~with access~~ is coupled to the bus in response to a control signal from the bus controller.

12. (Currently Amended) The system of Claim 11, wherein the bus controller allows simultaneous ~~access~~ coupling to the bus by a predetermined number of the plurality of processing devices in order to limit a load on the bus.

13. (Currently Amended) The system of Claim 11, wherein the bus controller receives a plurality of device access requests from the plurality of processing devices for ~~access~~ coupling to the bus.

14. (Currently Amended) The system of Claim 13, wherein the bus controller arbitrates the plurality of device access requests from the plurality of processing devices according to a predetermined protocol.

15. (Original) The system of Claim 11, wherein the bus is a PCI bus.

16. (Original) The system of Claim 15, wherein the PCI bus operates at a frequency of approximately 66 MHz.

17. (Currently Amended) A PCI bus, comprising:

a plurality of pass transistors, each pass transistor operable to provide coupling of an associated processing device ~~with bus access~~ to the bus, each pass transistor operable to receive a control signal to ~~enable and disable bus access for~~ couple and decouple its associated processing device to and from the bus.

18. (Original) The PCI bus of Claim 17, wherein a particular pass transistor receives an enable control signal in response to an access request sent by its associated processing device.

19. (Currently Amended) The PCI bus of Claim 17, wherein a particular pass transistor is operable to decouple ~~disable bus access for~~ its associated processing device from the bus such that the particular processing device does not appear to be coupled to the PCI bus in order to reduce a load on the bus.

20. (Original) The PCI bus of Claim 17, wherein each of the processing devices is operable to communicate at a 66 MHz rate.